

REMARKS

The Official Action dated September 7, 2005 has been received and its contents carefully noted. In view thereof, Applicant provides the following comments with respect thereto. As previously, claims 1-5 and 21-29 are presently pending in the instant application with claims 6-20 being withdrawn from further consideration by the Examiner has being drawn to a non-elected species.

Applicant hereby confirms the election of claims 1-5 and 21-29 for prosecution on the merits in the instant application.

With reference to paragraph 4 of the Office Action, claims 1, 3-5, 21, 23-26, 28 and 29 have been rejected under 35 U.S.C. §103 as being unpatentable over Applicant's admitted prior art ("Admission") in view of U.S. Patent No. 6,037,792 issued to McClure. This rejection is respectfully traversed in that the combination proposed by the Examiner neither discloses nor suggests that which is presently set forth by Applicant's claimed invention.

As discussed in Applicant's previous response, Applicant's claimed invention as recited in independent claim 1, is directed to a nonvolatile semiconductor memory device comprising a memory cell array having a plurality of memory cells and arranged in an array, the memory cells being connected to a plurality of bit lines and word lines, a plurality of address input terminals inputting a plurality of addresses thereto, a test mode circuit for outputting a test mode signal when a signal is inputted to a predetermined terminal among the address input terminals, a row decoder connected to the test mode circuit and applying an excess voltage for a test to all the word lines in response to the test mode signal, a column decoder connected to the test mode circuit and setting all the bit lines to a non-selecting state in response to the test mode signal and a monitor terminal connected to the test mode circuit for outputting the test mode signal. Similarly, independent claim 21 is directed to a

semiconductor memory device comprising a memory cell array having a plurality of memory cells, a plurality of word lines and a plurality of bit lines. A plurality of address input terminals for receiving a plurality of address signals is provided as well as a test mode circuit connected to the address input terminals, the test mode circuit providing a test mode signal in response to the address signals received thereto. Also provided is a row decoder connected to the test mode circuit and the memory cell array, the row decoder applying an excess voltage to all of the word lines in response to the test mode signal, a column decoder connected to the test mode circuit and the memory cell array, and a monitor terminal connected to the test mode circuit for outputting the test mode signal.

Independent claim 26 similarly recites a semiconductor memory device comprising a memory cell array having a plurality of memory cells, plurality of word lines and a plurality of bit lines, a plurality of address input terminals for receiving a plurality of address signals, a test mode circuit connected to the address input terminals, the test mode circuit providing a test mode signal in response to the address signals received thereto, a row decoder connected to the test mode circuit and the memory cell array, the row decoder applying an excess voltage to all of the word lines in response to the test mode signal, a column decoder connected to the test mode circuit and the memory cell, the column decoder receiving the test mode signal and a monitor pad connected to the test mode circuit for outputting the test mode signal. It is respectfully submitted that the combination proposed by the Examiner fails to disclose or suggest those features recited in each of independent claims 1, 21 and 26.

As noted hereinabove, the present invention relates to a semiconductor memory device having a monitor terminal for outputting a test signal. The test signal places the semiconductor memory device in a test mode. In this test mode, an excess voltage is applied to all of the word lines in response to the test mode signal. This test confirms defective

memory cells and removes such defective memory cells as is set forth in Applicant's specification at page 6, line 25 through page 7, line 13. Furthermore, in accordance with Applicant's claimed invention the test mode is monitored by the monitoring pad as noted from Applicant's specification at page 7, line 14 through page 8, line 13. Again, it is respectfully submitted that the combination proposed by the Examiner and particularly the teachings of Applicant's admitted prior art fails to disclose or remotely suggest those features in each of independent claims 1, 21 and 26.

In rejecting Applicant's claimed invention, the Examiner states that the Admissions discloses all the claimed elements except that the predetermined terminal is among the address input terminals and a monitor (or a pad) is connected to the test mode circuit and outputting the test mode signal. Applicant respectfully requests that the Examiner's position be reconsidered in that the Admission of Applicant clearly fail to disclose or suggest that which is described by the Examiner.

That is, as discussed in Applicant's specification, the conventional non-volatile semiconductor memory device is described in the second and third paragraphs of page 1 (Background Section). As discussed therein, the conventional non-volatile semiconductor memory device includes a test mode circuit, the test mode circuit applies a test mode voltage to all word lines in response to an exterior signal and that column switches are in a turning off state during the test mode. These features are significantly different from that which is presently set forth by Applicant's claimed invention.

While the Examiner may be corrected in stating that the bit lines, word lines and address input terminals are inherently disclosed, the Examiner's assertion that a test mode circuit for outputting a test mode signal is implied, for example, to control the selection of all word lines, is clearly incorrect and inconsistent with Applicant's Admissions. As noted

hereinabove, in the Background Section of the present specification, the test mode circuit is clearly set forth as applying the test mode voltage to all word lines, there is no description that the test mode circuit controls the selection of all word lines.

Further, in rejecting Applicant's claimed invention, the Examiner states that Applicant's Admissions implies that a row decoder is connected to the test mode circuit since all word lines are selected for testing. Again, Applicant respectfully submits that this is inconsistent with Applicant's Admissions and not inherent therein. Specifically, the Background Section of the present specification does not disclose a wave decoder at all. Additionally, the Background Section of the present specification fails to mention that all word lines are selected for testing. Furthermore, the Examiner appears to ignore the limitations set forth in each of the independent claims and that the column decoder is connected to the test mode circuit. Again, it is respectfully submitted that the Background Section of Applicant's specification wherein Applicant's Admissions are set forth, fails to disclose any form of a column decoder. Accordingly, it is respectfully submitted that the Examiner's interpretation of Applicant's Admissions is clearly inconsistent with that set forth in the Background portion of Applicant's specification. Furthermore, the patent to McClure fails to overcome the aforementioned shortcomings associated with Applicant's Admissions. Specifically, McClure discloses a semiconductor memory device having a flag terminal for outputting a burn-in stress test signal. The burn-in stress test is different from the oxide film stress test of the present invention. The Examiner appears to acknowledge this distinction in his response to Applicant's arguments. Accordingly, it is respectfully submitted that since the burn-in stress test does not relate to the row and column decoders and that McClure is silent with respect to the row and column decoders, Applicant's claimed invention as set forth

in each of independent claims 1, 21 and 26 clearly distinguish over the combination proposed by the Examiner and are in proper condition for allowance.

With respect to paragraph 5 of the Office Action, claims 2, 22 and 27 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art in view of McClure as applied to claims 1, 2 and 26 above and further in view of U.S. Patent No. 5,982,677 issued to Fontana et al. This rejection is likewise respectfully traversed in that the patent to Fontana et al. fails to overcome the aforementioned shortcomings associated with the prior art combination.

While Fontana et al. may disclose a select line connected to the drain of a memory cell connected to the select line and a circuit as well as giving a predetermined bias electric signal to the drain above the memory cell, this reference fails to overcome the aforementioned shortcomings associated with the prior combination of Applicant's admitted prior art and the teachings of McClure. Accordingly, it is respectfully submitted that each of claims 2, 22 and 27 which are directly dependent upon one of independent claims 1, 21 and 26 and include all the limitations thereof clearly distinguish over the combination proposed by the Examiner and are in proper condition for allowance.

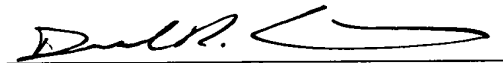
With respect to paragraph 6 of the Office Action and particularly the Examiner's response to Applicant's previous arguments, it is respectfully submitted that the foregoing comments clarify Applicant's position with respect to the prior art cited by the Examiner and particularly the Examiner's interpretation of Applicant's Admission set forth in the Background portion of the present specification. Again, it is noted that McClure discloses a semiconductor memory device having a flag terminal for outputting a burn-in stress test signal. The burn-in stress test is different from the oxide film stress test of the present invention. Once again, the Examiner appears to acknowledge this distinction in his response

to Applicant's arguments. Accordingly, it is respectfully submitted that since the burn-in stress test does not relate to the row and column decoders and that McClure is silent with respect to the row and column decoders, it is respectfully submitted that Applicant's claimed invention clearly distinguishes over the teachings of Applicant's Admissions in view of McClure and is in proper condition for allowance.

Therefore, in view of the foregoing it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that claims 1-5 and 21-29 be allowed and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,



Donald R. Studebaker  
Reg. No. 32,815

Nixon Peabody LLP  
401 9<sup>th</sup> Street N.W.  
Suite 900  
Washington, D. C. 20004  
(202) 585-8000